UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/068,326	02/06/2002	Benny W.H. Lai	10004400-1	8823

57299 7590 03/07/2006

AVAGO TECHNOLOGIES, LTD.
P.O. BOX 1920
DENVER, CO 80201-1920

EXAMINER	
TABONE JR, JOHN J	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 03/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/068,326	LAI, BENNY W.H.	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-15 and 17-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-15 and 17-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

FINAL DETAILED ACTION

1. Claims 1-4, 6-15 and 17-19 remain in this application. Claim 15 has been amended. Claims 5, 16 and 20 have been cancelled.

Response to Arguments

2. Applicant's arguments filed 12/07/2005 for claims 1 and 9 have been fully considered but they are not persuasive. Also, Applicant's arguments with respect to claim 15 have been considered but are moot in view of the new ground(s) of rejection.

As per arguments for independent claims 1and 9:

Applicant's main arguments for these claims appear to the Examiner to be based that "Takinosawa does not teach a plurality of functionally identical testers" and "Douskey does not teach or suggest a plurality of functionally identical testers". Also, "Douskey does not teach an FTI associated with each SERDES". The Examiner would like to point out that it is the combination of Takinosawa and Douskey as set forth in the previous Office Action of Record that teaches "a plurality of functionally identical testers" and "an FTI associated with each SERDES". Takinosawa teaches a "functionally identical tester" and an FTI associated with a single SERDES. The Examiner asserts that integrating Takinosawa's SERDES as well as the built-in self-test circuit (TX-BIST) circuit 35, a multiplexer 36, a built-in self-test analyzer circuit 49 (**functionally identical tester**) into Douskey's CIU's 62 (**said testers**) enables Takinosawa to test a plurality of SERDESs which includes a plurality of functionally identical testers. It is a total

replacement of Douskey's CIU's 62 not a kludge as the Applicant suggests on page 8, 3rd paragraph to page 9, 2nd paragraph and page 10, 1st paragraph. Further, Douskey suggests that the invention should not be limited to use with any particular design or end use of an integrated circuit device and that a core may be custom designed for a particular design, or may be reused from a previous design, whether generated internally within a business entity or licensed from another entity. Moreover, a core may be considered to include any custom circuit arrangement that is required to integrate together or extend the functionality of existing core designs for use in a particular custom design. (Col. 5, ll. 63-67; col. 6, ll. 24-31, 35-47, Fig. 2).

It is the Examiner's conclusion that independent claims 1 and 9 are not patentably distinct or non-obvious over the prior arts of record namely, Takinosawa (US-2003/0035473) in view of Douskey et al. (US-6115763). Therefore, the rejection is maintained. Based on their dependency on independent claims 1 and 9, claims 2-4 and 6-8, 10-14, respectively, stand rejected.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-4,6-15 and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takinosawa (US-2003/0035473), hereinafter Takinosawa in view of Douskey et al. (US-6115763), hereinafter Douskey.

Claim 1:

Takinosawa teaches "**serializer/deserializers (SERDESs) and core processing logic integrated with each said SERDES and connected to each said SERDES to exchange signals**" in that the USB physical layer 18 (of the USB layer 17) functions to convert the parallel data received from the USB link layer 16 (of the USB layer 17) (**core processing logic**) into a serial format (**serializer**) and converts the data to a parallel format (**deserializer**) and transmits the data to the USB link layer 16 via a data bus 25. Takinosawa also teaches the data to be transmitted is first provided by the microcontroller 12 to the USB link layer 16 (**core processing logic**). Takinosawa further teaches "**functionally identical testers integrated with said plurality of SERDESs and said core processing logic, said testers being connected to individually test each said SERDESs**" in that the USB physical layer 18 comprises a built-in self-test circuit (TX-BIST) circuit 35, a multiplexer 36, a built-in self-test analyzer circuit 49 (**functionally identical tester**). (Page 2, ¶s 22-24, Figs. 1 and 2). Takinosawa does not explicitly teach "**a plurality of SERDESs**", "**a plurality of functionally identical testers**" and "**each said tester is connected to a common test bus that is integrated with said SERDESs and said testers**". Douskey teaches in an analogous art integrated circuit device 50 generally includes a plurality of cores 60 (**a plurality of SERDESs and a plurality of functionally identical testers**) interconnected together

via one or more functional interfaces, e.g., functional interface 51 utilizing bus 52. Bus 52 is coupled to an external interface such as the system bus via a system interface unit (SIU) 54 having an external function access port 54a (used during normal mode). Douskey suggests that the invention should not be limited to use with any particular design or end use of an integrated circuit device and that a core may be custom designed for a particular design, or may be reused from a previous design, whether generated internally within a business entity or licensed from another entity. Moreover, a core may be considered to include any custom circuit arrangement that is required to integrate together or extend the functionality of existing core designs for use in a particular custom design. (Col. 5, ll. 63-67; col. 6, ll. 24-31, 35-47, Fig. 2). Douskey further teaches "**each said tester is connected to a common test bus that is integrated with said SERDESs and said testers**" in that a service interface 55 for providing service functions (See col. 6, l. 65 to col. 7, l. 16) generally includes a bus 56 (**common test bus**) which couples a master interface unit (MIU) 58 (I/O tester controller of claim 6) to a plurality of core interface units (CIU's) 62 (**said testers**) disposed in each of cores 60. MIU 58 is principally used to pass requests received externally from device 50 to one or more of CIU's 62 (**said testers**) so that predetermined service operations are performed by the CIU's (**said testers**) as required. (Col 7, ll. 17-23, Fig 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to repeat Takinosawa's USB layer 17 as in Douskey's integrated circuit device 50, which includes a plurality of cores 60. It also would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate Takinosawa's

built-in self-test circuit (TX-BIST) circuit 35, a multiplexer 36, a built-in self-test analyzer circuit 49 (**functionally identical tester**) into Douskey's CIU's 62 (**said testers**). The artisan would be motivated to do so because this would enable Takinosawa to test a plurality of SERDESs which includes a plurality of functionally identical testers. The artisan would also be motivated to do so because then the a plurality of SERDESs and plurality of functionally identical testers would share a common bus for distributing test data to the plurality of functionally identical testers. Douskey teaches in an analogous art "**each of said testers being enabled to detect performance characteristics of individual said SERDESs independently of other said testers**" and "**each said tester having a unique address that enables independent accessibility of said tester via said test bus**" in that to initiate a READ operation, master interface unit 72 (I/O tester controller of claim 6) first drops IDLE signal 90, and thereafter the ADDR lines at 93 are driven to a predetermined address including the base address of the target CIU (**said tester**), as well as a unique address therein, e.g., corresponding to a specific register in that CIU (**said tester**). Douskey illustrates in FIG. 3, each CIU includes a base address supplied thereto, which uniquely identifies the CIU on the bus. Douskey also teaches once the ADDR lines 93 are stabilized, MIU 72 initiates a READ operation by asserting READ line 91. Each CWU then samples the ADDR lines and decodes the base address to determine whether the request is directed to that particular CIU (**said tester**). (Col. 8, ll. 43-61).

Claim 2:

Takinosawa teaches a peripheral device 10 (semiconductor substrate) comprises a microcontroller 12 (core processing logic), an application layer 14, a USB link layer 16 (core processing logic) and a USB physical layer 18 (SERDESs and testers). (Page 2, ¶ 20).

Claims 3:

Takinosawa teaches when TX-BIST enable signal is active, the TX-BIST circuit 35 (functional test interface (FTI)) functions to generate a series of pseudo random data words, which are output by the TX-BIST circuit 35 and coupled to the holding register 37 via the multiplexer 36 (tester controller). Takinosawa discloses that multiplexer 36 (tester controller) is controlled via the TX-BIST enable signal (select operational modes) to select between the data bus 21 (normal mode) or the output of the TX-BIST circuit 35 (tester interface) (BIST mode) as an input. (Page 3, ¶ 25 and 28, Fig. 2).

Claims 4:

Takinosawa teaches when TX-BIST enable signal is active, the TX-BIST circuit 35 (tester interface) functions to generate a series of pseudo random data words (test pattern generator) and is connected to the parallel data on data bus 21. Takinosawa also teaches The BIST analyzer circuit 49 (error detector), whose input is coupled to the output of the holding register 48 and receives the decoded, unstuffed test data via the bus 25 (parallel data from SERDES), then functions to compare the received test data with the known test data generated by the TX-BIST circuit 35 and generate an error if the expected data is not received. (Page 3, ¶ 28, Page 4, ¶ 31, Fig. 2).

Claims 6:

Douskey teaches "**an input/output tester controller integrated with said SERDESs and said testers, said input/output tester controller being coupled between said test bus and an output of said integrated circuit for signal communication with an external source for sequencing test operations**" in that MIU 110 (**input/output tester controller)** is also coupled to a service bus (**test bus)** implemented in this embodiment as a JTAG IEEE standard 1149.1 interface. Douskey also discloses using the core service interface 70 of FIG. 3, built-in test operations may be executed in response to commands supplied from an external access port to master interface unit 72 (**signal communication with an external source**). For example, if master interface unit 72 is, coupled to a JTAG-compatible test access port (TAP) JTAG-compatible commands may be issued to specific core interface units via MIU 72. (Col. 10, ll. 40-51).

Claims 7:

Takinosawa teaches that the USB physical layer 18 (SERDES) comprises a built-in self-test circuit (TX-BIST) circuit 35 (tester comprising a BIST state machine), a multiplexer 36, a built-in self-test analyzer circuit 49 (plurality of testers) and is connected to the data bus 21 (test bus). (Page 2, ¶ 24, Fig. 2).

Claim 8:

Takinosawa teaches when TX-BIST enable signal is active, the TX-BIST circuit 35 (tester) functions (responsive to individual commands) to generate a series of pseudo random data words (individually but concurrently operated), which are output by

the TX-BIST circuit 35 and coupled to the holding register 37 via the multiplexer 36 (tester). (Page 3, ¶ 28).

Claim 9:

Takinosawa teaches "**serializer/deserializers (SERDESs) and core circuitry integrated on the substrate each said SERDES having parallel data inputs and parallel data outputs and having serial data inputs and outputs**" in that the USB physical layer 18 (of the USB layer 17) functions to convert the parallel data received from the USB link layer 16 (of the USB layer 17) (**core processing logic**) into a serial format (**serializer**) and converts the data to a parallel format (**deserializer**) and transmits the data to the USB link layer 16 via a data bus 25. Takinosawa also teaches the data to be transmitted is first provided by the microcontroller 12 to the USB link layer 16 (**core processing logic**). Takinosawa further teaches "**functional test interfaces (FTIs) integrally formed with said substrate, each said FTI being uniquely associated with one of said SERDESs and being connected to said parallel data inputs and outputs of said associated SERDES**" and "**functional test controllers (FTCs) integrally formed with said substrate, each said FTC being uniquely associated with one of said FTIs and being configured to select among operational modes of said associated FTI**" in that the USB physical layer 18 comprises a built-in self-test circuit (TX-BIST) circuit 35 (**FTC**), a multiplexer 36 (**FTI**), a built-in self-test analyzer circuit 49. (Page 2, ¶s 22-24, Figs. 1 and 2). Takinosawa does not explicitly teach "**a plurality of SERDESs**", "**a plurality of FTIs**", "**a plurality of FTCs**" and "**a common test bus integrally formed with said substrate, said**

common test bus being dedicated to providing signaling for enablement of testing". Douskey teaches in an analogous art integrated circuit device 50 generally includes a plurality of cores 60 (**a plurality of SERDESs , a plurality of FTIs, a plurality of FTCs**) interconnected together via one or more functional interfaces, e.g., functional interface 51 utilizing bus 52. Bus 52 is coupled to an external interface such as the system bus via a system interface unit (SIU) 54 having an external function access port 54a (used during normal mode). Douskey suggests that the invention should not be limited to use with any particular design or end use of an integrated circuit device and that a core may be custom designed for a particular design, or may be reused from a previous design, whether generated internally within a business entity or licensed from another entity. Moreover, a core may be considered to include any custom circuit arrangement that is required to integrate together or extend the functionality of existing core designs for use in a particular custom design. (Col. 5, ll. 63-67; col. 6, ll. 24-31, 35-47, Fig. 2). Douskey further teaches "**a common test bus integrally formed with said substrate, said common test bus being dedicated to providing signaling for enablement of testing**" in that a service interface 55 for providing service functions (See col. 6, l. 65 to col. 7, l. 16) generally includes a bus 56 (**common test bus**) which couples a master interface unit (MIU) 58 (I/O tester controller) to a plurality of core interface units (CIU's) 62 (**a plurality of FTIs, a plurality of FTCs**) disposed in each of cores 60. MIU 58 is principally used to pass requests received externally from device 50 to one or more of CIU's 62 (**a plurality of FTIs, a plurality of FTCs**) so that predetermined service operations are performed by

the CIU's (**a plurality of FTIs**, **a plurality of FTCs**) as required. (Col 7, ll. 17-23, Fig 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to repeat Takinosawa's USB layer 17 as in Douskey's integrated circuit device 50, which includes a plurality of cores 60. It also would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate Takinosawa's built-in self-test circuit (TX-BIST) circuit 35, a multiplexer 36, a built-in self-test analyzer circuit 49 (**a plurality of FTIs**, **a plurality of FTCs**) into Douskey's CIU's 62 (**a plurality of FTIs**, **a plurality of FTCs**). The artisan would be motivated to do so because this would enable Takinosawa to test a plurality of SERDESs which includes a plurality of functionally identical testers. The artisan would also be motivated to do so because then the a plurality of SERDESs and plurality of functionally identical testers would share a common bus for distributing test data to the plurality of functionally identical testers. Douskey teaches in an analogous art "**said FTIs being enabled to individually and concurrently test performances of said SERDESs**" and "**said IOC being connected to each said FTC via said common test bus to transmit individually addressed commands to each said FTC**" in that to initiate a READ operation, master interface unit 72 (**I/O tester controller**) first drops IDLE signal 90, and thereafter the ADDR lines at 93 are driven to a predetermined address including the base address of the target CIU (**FTI**, **FTC**), as well as a unique address (**individually addressed commands**) therein, e.g., corresponding to a specific register in that CIU (**FTI**, **FTC**). Douskey illustrates in FIG. 3, each CIU includes a base address supplied thereto, which uniquely identifies the CIU on the bus. Douskey also teaches once the ADDR lines 93 are

stabilized, MIU 72 initiates a READ operation by asserting READ line 91. Each CWU then samples the ADDR lines and decodes the base address to determine whether the request is directed to that particular CIU (**FTI**, **FTC**). (Col. 8, ll. 43-61). Douskey also teaches "**an input/output controller (IOC) and common test bus integrally formed with said substrate**" and "**said IOC further being connected to exchange signals with an external device**" in that MIU 110 (**IOC**) is also coupled to a service bus (**common test bus**) implemented in as a JTAG IEEE standard 1149.1 interface wherein using the core service interface 70 of FIG. 3, built-in test operations may be executed in response to commands supplied from an external access port to master interface unit 72. Douskey further teaches if master interface unit 72 is, coupled to a JTAG-compatible test access port (TAP) JTAG-compatible commands may be issued to specific core interface units (**individually addressed commands**) via MIU 72 (**IOC**). (Col. 10, ll. 40-51, Fig. 2 and 7).

Claim 15:

Takinosawa in view of Douskey as per the rejections of claims 1 and 9 substantially teaches embedding a plurality of test interfaces within said integrated circuit such that each test interface is specific to one said SERDES with respect to exchanging parallel data, embedding test controllers within said integrated circuit such that each said test controller is specific to one said test interface with respect to triggering test operations by said test interface, providing an integrated circuit output that enables said test controllers to be individually addressed, and embedding an input/output controller (IOC) and a test bus within said integrated circuit, including

connecting said IOC between said integrated circuit output and said test bus and including linking each said test controller to said test bus. Takinosawa teaches when TX-BIST enable signal is active, the TX-BIST circuit 35 (tester interface) functions to generate a series of pseudo random data words (test pattern generator) and is connected to the parallel data on data bus 21. Takinosawa also teaches The BIST analyzer circuit 49 (error detector), whose input is coupled to the output of the holding register 48 and receives the decoded, unstuffed test data via the bus 25 (parallel data from SERDES), then functions to compare the received test data with the known test data generated by the TX-BIST circuit 35 and generate an error if the expected data is not received. (Page 3, ¶ 28, Page 4, ¶ 31, Fig. 2).

Claim 10:

Takinosawa further teaches when TX-BIST enable signal is active, the TX-BIST circuit 35 (functional test interface (FTI)) functions to generate a series of pseudo random data words, which are output by the TX-BIST circuit 35 and coupled to the holding register 37 via the multiplexer 36 (tester controller). Takinosawa discloses that multiplexer 36 (tester controller) is controlled via the TX-BIST enable signal (select operational modes) to select between the data bus 21 (normal mode) or the output of the TX-BIST circuit 35 (tester interface) (BIST mode) as an input. (Page 3, ¶ 25 and 28, Fig. 2).

Claim 11:

Takinosawa teaches when TX-BIST enable signal is active, the TX-BIST circuit 35 (tester interface) functions to generate a series of pseudo random data words (test

pattern generator) and is connected to the parallel data on data bus 21. Takinosawa also teaches The BIST analyzer circuit 49 (error detector), whose input is coupled to the output of the holding register 48 and receives the decoded, unstuffed test data via the bus 25 (parallel data from SERDES), then functions to compare the received test data with the known test data generated by the TX-BIST circuit 35 and generate an error if the expected data is not received. (Page 3, ¶ 28, Page 4, ¶ 31, Fig. 2).

Claims 12 and 18:

Takinosawa teaches that the USB physical layer 18 (SERDES) comprises a built-in self-test circuit (TX-BIST) circuit 35 (tester comprising a BIST state machine), a multiplexer 36, a built-in self-test analyzer circuit 49 (plurality of testers) and is connected to the data bus 21 (test bus). (Page 2, ¶ 24, Fig. 2).

Claim 13:

Takinosawa in view of Douskey as per the rejections of claims 1 and 9 teaches each of said FTIs (CIUs 62) is connected to said IOC (master interface unit 58 (MIU)) via a common test bus (bus 56, Fig. 2), said FTIs also being connected to said core circuitry.

Claim 14:

Takinosawa in view of Douskey as per the rejections of claims 1 and 9 teaches each said FTI (CIUs 62) is assigned a unique address, said IOC (master interface unit 58 (MIU)) being enabled to individually manipulate said FTIs by employing said unique addresses in that to initiate a READ operation, master interface unit 72 (**IOC**) first drops IDLE signal 90, and thereafter the ADDR lines at 93 are driven to a predetermined

address including the base address of the target CIU (**FTI**), as well as a unique address (**individually addressed commands**) therein, e.g., corresponding to a specific register in that CIU (**FTI**). Douskey illustrates in FIG. 3, each CIU includes a base address supplied thereto, which uniquely identifies the CIU on the bus. Douskey also teaches once the ADDR lines 93 are stabilized, MIU 72 initiates a READ operation by asserting READ line 91. Each CWU then samples the ADDR lines and decodes the base address to determine whether the request is directed to that particular CIU (**FTI**). (Col. 8, ll. 43-61).

Claim 17:

Takinosawa teaches when TX-BIST enable signal is active, the TX-BIST circuit 35 functions (enabling all test interfaces) to generate a series of pseudo random data words, which are output by the TX-BIST circuit 35 and coupled to the holding register 37 via the multiplexer 36 (test controller). Takinosawa also teaches The BIST analyzer circuit 49 (tester), whose input is coupled to the output of the holding register 48 and receives the decoded, unstuffed test data via the bus 25, then functions to compare the received test data with the known test data generated by the TX-BIST circuit 35 and generate an error if the expected data is not received (monitor performance of SERDES). (Page 3, ¶ 28, Page 4, ¶ 31).

Claim 19:

Douskey does not explicitly teach the step of forming an insulative package to house circuitry of said integrated circuit. However, Douskey does suggest this limitation in that device 50 generally includes a plurality of cores 60 interconnected together via

one or more functional interfaces, e.g., functional interface 51 utilizing bus 52. Bus 52 is coupled to an external interface such as the system bus via a system interface unit (SIU) 54 having an external function access port 54a. (Col. 6, ll. 24-31). It would have been obvious to one of ordinary skill in the art at the time the invention was made to that Douskey's integrated circuit device 50 is housed in an insulative package. The artisan would be motivated to do so because ICs which communicate with an external device are in package form.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John J. Tabone, Jr. 3/2/06
Examiner
Art Unit 2138

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100